FIELD ANALYSIS AND DESIGN CRITERIA FOR T-GATE TW-FET'S WITH POSITIVE GAIN

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ABSTRACT

We present an accurate e.m model of T-Gate TW-FET's and necessary conditions for obtaining exponentially growing waves.
This model takes into detailed account device geometry, the effect of carrier velocity saturation in the high field region, conductor and dielectric losses and small signal channel current.

INTRODUCTION

The quest for solid-state devices exploiting the interaction between carriers and propagating wave in order to achieve the wide-band advantages typical of TWTs (Traveling Waves Tubes) is far from recent.
A wealth of contributions have approached the subject of TW-FET's from the circuit point of view, employing field approximations that are now considered unacceptable in the light of subsequent full wave analysis of propagation phenomena in structures with large losses. Electromagnetically rigorous models of active devices have been proposed in [1] and [2].The absence of a clear picture of the single device distributed amplifier, is borne out by the scarcity of experimental work reporting growing wave phenomena in TW-FET [3,4]. In this contribution, we propose a substantial evolution of the model proposed by ourselves in [2] with application to a T-Gate device and highlight a set of design guidelines.

ANALYSIS

The following integral equation holds for the current $\bar{J}$ in the conducting regions [2]:

$$\left[\tilde{G}(r,r')\bullet\tilde{Z}(r',r'')+\sigma(r)\,\tilde{Z}(r,r'')+\tilde{I}(r,r'')\right]\bullet\bar{J}(r'')=0\,;\quad r,r''\in\Sigma_p\cup\Sigma_a \tag{1}$$

where Σ_p is the set of passive conducting regions, Σ_a is the set of active ones. $\tilde{\mathbf{Z}}$ is the dyadic Green function of the multilayer dielectric substrate, $\tilde{\mathbf{G}}$ the dyadic operator describing the control mechanism of the carrier flow in the channel, σ the conductivity of the spatially limited conducting regions.
Unlike in [2], we now utilize the following model for $\tilde{\mathbf{G}}$

$$\tilde{G}(r,r')=\frac{g_m}{L\,d}e^{-j\omega\tau}\,\delta(x')\,e^{-\gamma(z-z')}\,\hat{x}\hat{y} \tag{2}$$

where r belongs to the channel and r' to the region below the gate electrode.
In (2) g_m is the small signal transconductance, L the device length, d the effective channel width (i.e. without the depletion depth) and τ is the carrier transit time.
The above choice is tantamount to assuming the voltage across the depletion layer as control voltage. Moreover the channel is now divided into two regions: a high conductivity one where σ is of the order of 10000 S/m, modelling the low static field region, and a high conductivity one (~200-400 S/m), where the carriers proceed with saturation drift velocity; such a situation is common to most currently used GaAs devices.

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POWER CONSIDERATIONS AND DESIGN GUIDELINES

In order for a wave impinging in the channel to gain energy from it, Poynting's theorem requires that at any arbitrary section we have:

$$\overline{P}_{ch} = Re \iint_{ch} dx\, dy\, \overline{\mathbf{E}} \cdot \overline{\mathbf{J}}^{*}_{ch} < 0 \qquad (3)$$

The most general form for the channel current $\overline{\mathbf{J}}_{ch}$, as used in (1), is:

$$\overline{J}_{ch}(r) = \tilde{G}(r,r') \bullet \overline{E}(r') + \sigma_{ch}\, \overline{E}(r); \qquad (3a)$$

where σ_{ch} is the channel conductance. Consequently, from (3) we find

$$Re\left\{ \iint_{ch} dx\, dy\, \overline{\mathbf{E}} \cdot \tilde{\mathbf{G}}^{*} \overline{\mathbf{E}}^{*} + \sigma_{ch} |\overline{\mathbf{E}}|^{2} \right\} < 0 \qquad (4)$$

showing the advantage of HEMT structures where σ_{ch} too is low. From (4) by adopting $\tilde{\mathbf{G}}$ as given in (2), and setting, with reference to Fig.2,

$$\overline{\mathbf{E}}(\mathbf{r}) = \mathbf{e}(x,y)\, e^{-\gamma z}$$

$$\iint_{ch} dx\, dy\, e_x(x,y) \cong -d\, V_{ds}$$

$$-V_{gh} \overset{\Delta}{=} \int_{-H}^{0} dy'\, e_y(0,y')$$

we obtain:

$$Re\left\{ V_{ds}\, V_{gh}^{*}\, e^{j\omega\tau} \right\} < 0 \qquad (5)$$

Hence, since $V_{ds} = V_{gs} + V_{dg}$ and $V_{gh} = V_{gs} - V_{hs}$, (5) yields

$$Re\left\{ \left[V_{dg}\, V_{gs}^{*} - V_{hs}^{*}\, (V_{dg} + V_{gs}) \right] e^{j\omega\tau} \right\} < 0 \qquad (6)$$

leading to the following considerations:
a) the mode commonly defined in [1] as "gate-mode" is capable of gain (see Fig.1);
b) the "bulk mode" is rather insensitive to channel current since $\mathbf{E} \cdot \mathbf{J}_{ch} \approx 0$;
c) in a physically symmetric structure, such as the one proposed in [1], for the gate-mode where $V_{ds} \cong 0$ so that $V_{ds} V_{gh}^{*} \approx 0$, and there is hardly any interaction between channel and travelling wave, as observed in [9]: this, however, is just a consequence of having assumed the channel conductivity as homogeneous;

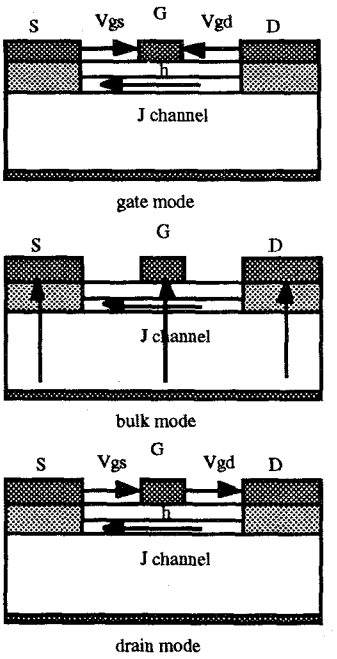

Fig. 1: voltage configuration and channel current for the three modes in a symmetric FET structure.

d) in a symmetric structure $V_{gh} \cong 0$ for the drain-mode, so that this too is insensitive to variations of g_m: the results of [1] and [2] concerning a deterioration of losses for increasing g_m values are a consequence of the choice of control voltage.
In fact, by selecting V_{gs} as control voltage, (4) gives (neglecting the transit time):

$$Re\left\{ V_{ds}\, V_{gs}^{*} \right\} < 0 \qquad (7)$$

but the L.H.S. quantity above is, at most, positive in the drain-mode, as V_{ds} and V_{gs} point the same way.

Design Criteria

1) Asymmetric structures are better suited to obtaining gain;

2) the field between G and D is to be maximized in order to increase the correlation between incident field and channel current where their phases are in opposition. This remark agrees with the results of the analysis of [5] on the effect of the gate-drain capacitance.
3) A correct phase-velocity equalization is required for the gate and drain electrodes in order for (5) to be satisfied in the gate-mode: it is necessary that the phase-velocities of the gate-source mode and that of the drain-source mode, considered as decoupled, be similar.
This consideration justifies adding capacitance between drain and source, as proposed in [3], in order to compensate for the high capacitance underneath the gate electrode, or even adopting drain electrodes of large dimensions, as in [6], as these modifications comply with all points 1) to 3) above. Moreover, for higher frequencies, the carrier transit time can play an important role in phase equalization.
4) Ohmic losses reduce phase velocity [7], making phase equalization critical, particularly with regard to the gate electrode. The adoption of a T-gate seems therefore mandatory.

SIMULATIONS AND RESULTS

Fig.2 shows, just as an example, a structure similar to that proposed in [6] apart from the width of the n^+ regions, that appeared to be in contrast with requirement 2) above.

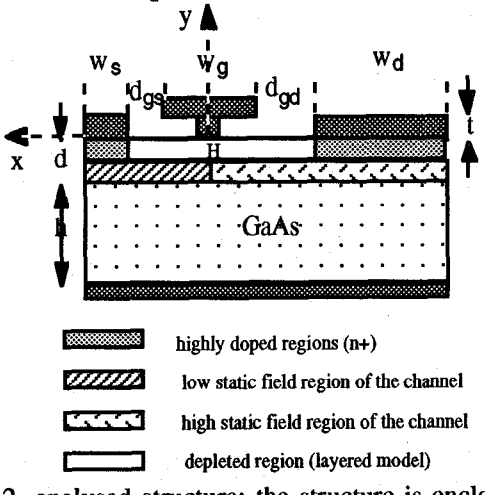

Fig. 2- analysed structure: the structure is enclosed in a large metallic box (not shown: box width 600μm); w_S= 2μm; d_{gs}= 10μm; w_g= 30μm; base of gate 1μm; d_{gd}= 100μm; w_d= 300μm; t= 1μm; t (T-bar)= 1μm; h= 29.8μm; d= 0.2μm; depletion depth 0.15μm; ε_r= 12.9; strips and ground conductivity 3 10^7 S/m; highly doped regions conductivity 2 10^5 S/m; the low-field conductivity of the channel is 10000 S/m, corresponding to N_D= 7.5 10^{22} atoms/m^3 and μ_n= 8500 cm^2/V sec; the high-field conductivity is assumed 400 S/m; transit time τ=4pS.

The device is biased near pinch-off in order to reduce gate capacity, consistently with the principle under 3). Nevertheless this bias reduces the transconductance, so that a trade-off is needed in practical devices; in our simulations we assume given transconductance values, without describing this effect. In Fig.3 we report the dispersion curves for vanishing transconductance, whereas that of a device having g_m=100 mS and 1 mm length is reported in Fig.4. Due to the asymmetry, we use the mode definition of [2], with reference to the relative current density distribution at the electrodes.

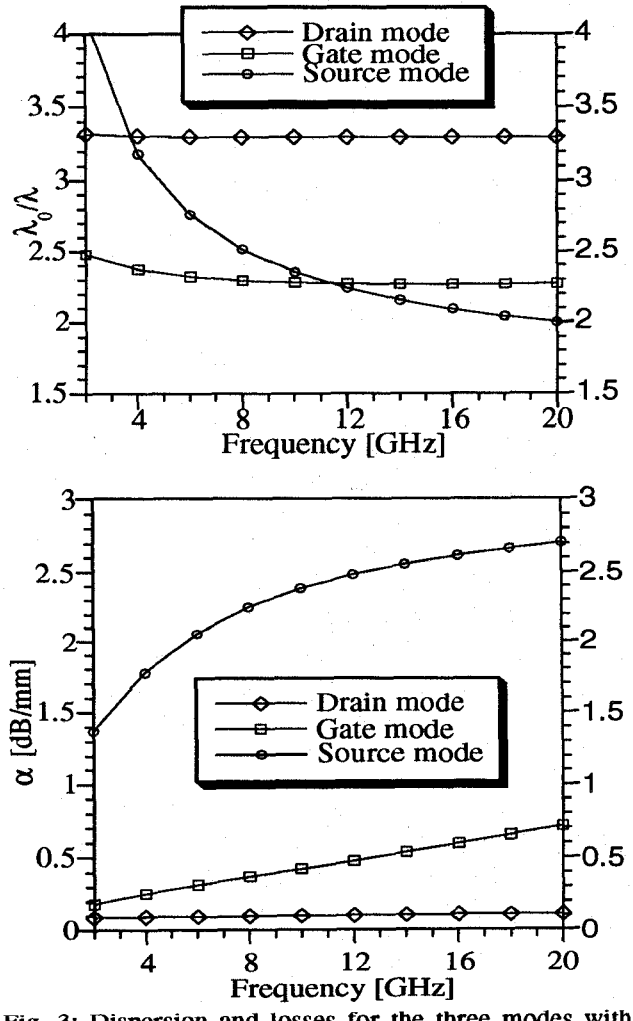

Fig. 3: Dispersion and losses for the three modes with g_m=0; due to the asymmetry, modes are defined according to the maximum of current distribution in each metal strip.

Drain and source-modes are slightly affected by the presence of a transconductance: the small signal current increases drain-mode losses while reducing source-mode losses.

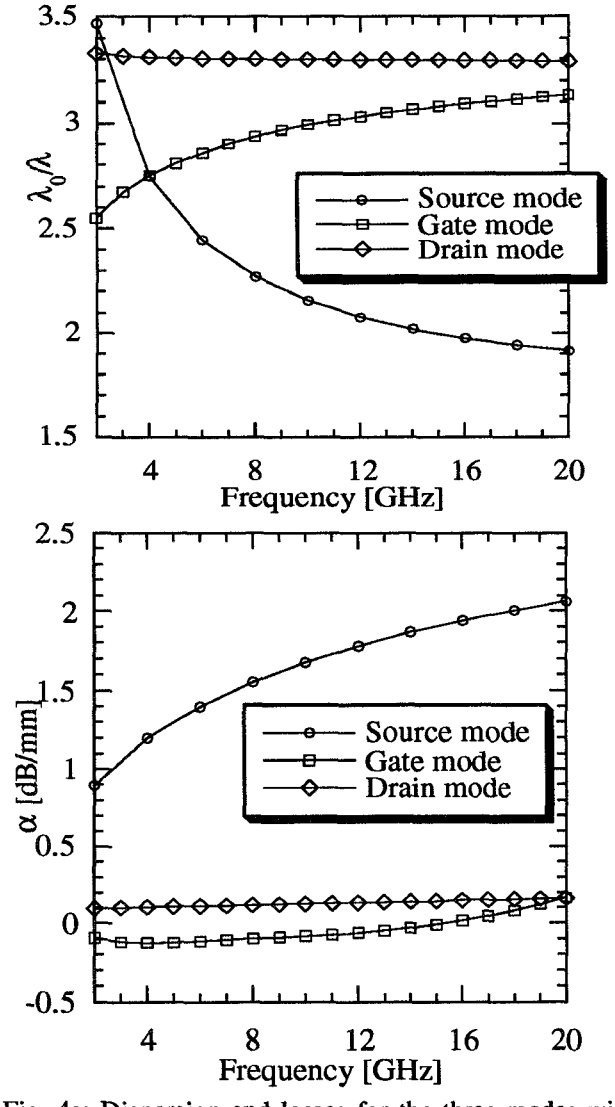

Fig. 4a: Dispersion and losses for the three modes with g_m=100 mS: the attenuation factor of the gate-mode becomes negative, describing an exponentially growing wave.

On the other hand, the attenuation constant of the gate-mode becomes negative over a certain range of frequencies. The actual gain is band-limited by transconductance cut-off phenomena.

CONCLUSIONS

We propose a full-wave model of T-gate TW-FET's that includes detailed account of geometry, the effect of carrier velocity saturation, finite electrode conductivity and dielectric losses as well a small signal gain.

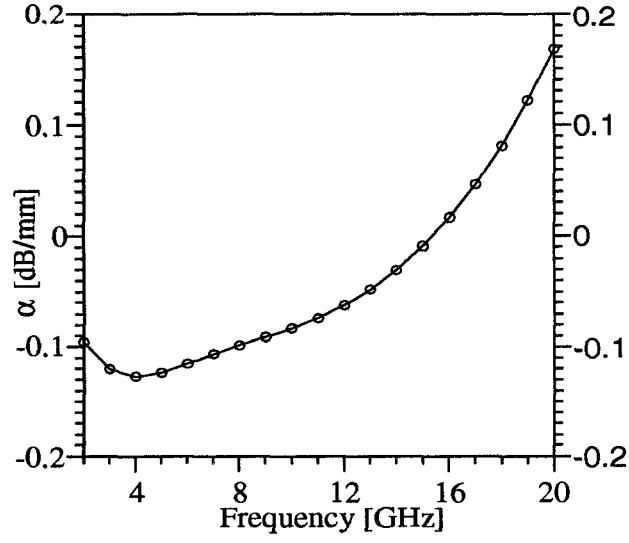

Fig. 4b: Detail of the gain region of the gate mode.

Several design principles emerge from basic power considerations, confirming previous experiments and suggesting ways of optimizing the structure.

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